I. GENERAL INFORMATION

This section provides general information on the AX700E/ES VHF/UHF wideband receivr AX700E/ES.

- Indicated frequency is divided into the following four (4) band zone by B1, B2, B3, and BU terminals of tuners (P053).

  B1 ..... 50.00 to 87.75 MHz
  B2 ..... 95.75 to 215.75 MHz
  B3 ..... 221.75 to 473.75 MHz
  BU ..... 475.75 to 904.995 MHz

- The following three modes have been programmed into the demoudulator, from which one mode can be selected.

  RM-W (wide),
  FM-N (narrow)
  AM

- There are six channel steps: 5 (AJ = Fine Adjustable), 1 (UP/DOWN key), 10, 12.5, 20, and 25 kHz.

- Reception systems are as follows:

  FM-W ..... Double conversion superheterodyne system
  First IF ..... 46 MHz
  Second IF ..... 10.7 MHz
  Third IF ..... 455 KHz

  FM-N/AM ..... Triple conversion superheterodyne system
  First IF ..... 46 MHz
  Second IF .... 10.7 MHz
  Third IF ..... 455 kHz

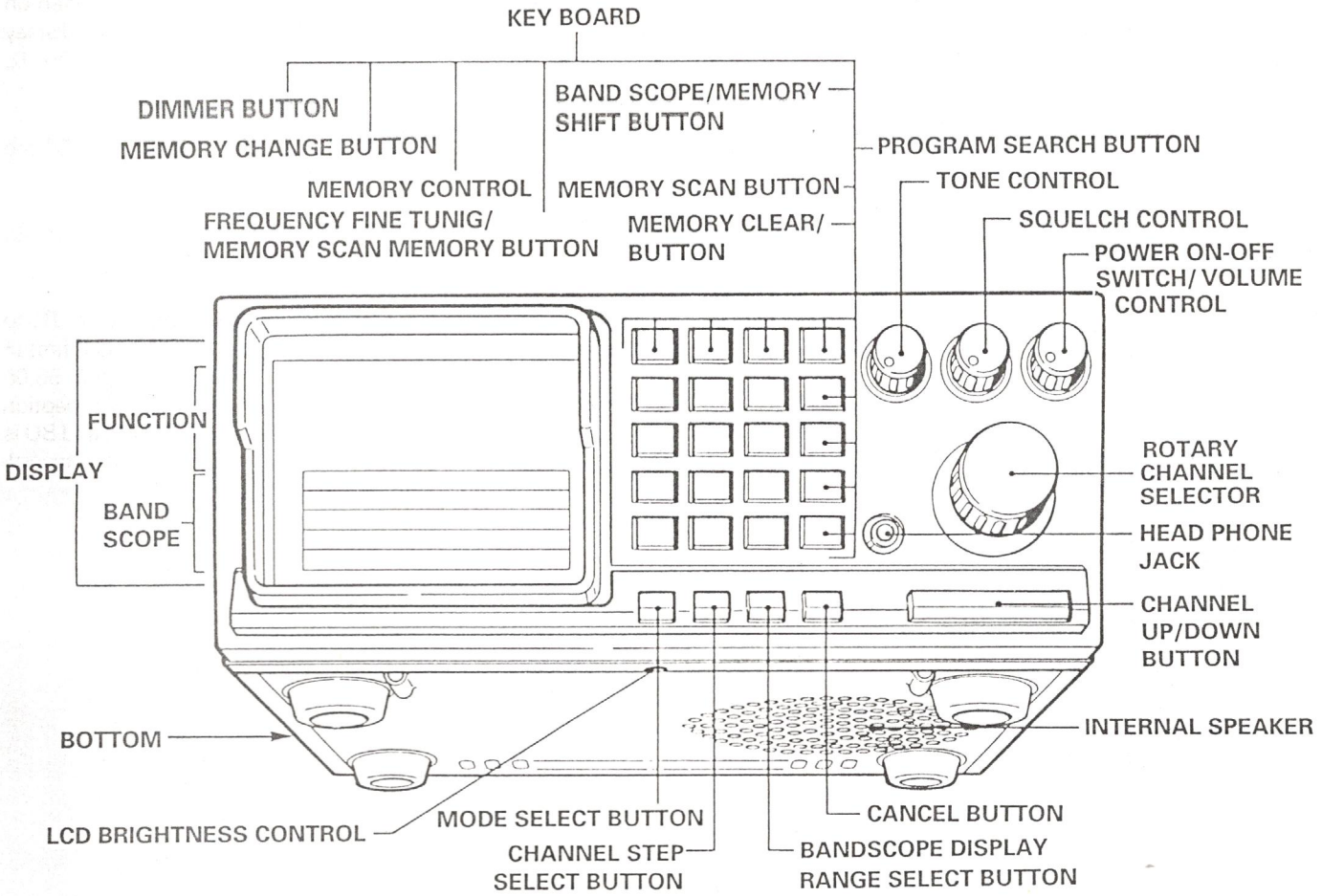
- The spectrum level on the band scope (spectrum analyzer) is displayed by the digital conversion of the level detection output. The adjustment of the signal intensity (S) on the bandscope for the maximum level "0V" (S11) is based on the intensity of an incoming signal of 60 dBμV. The display width of the bandscope can be set to 1 MHz, 250 (260) kHz, or 100 kHz.

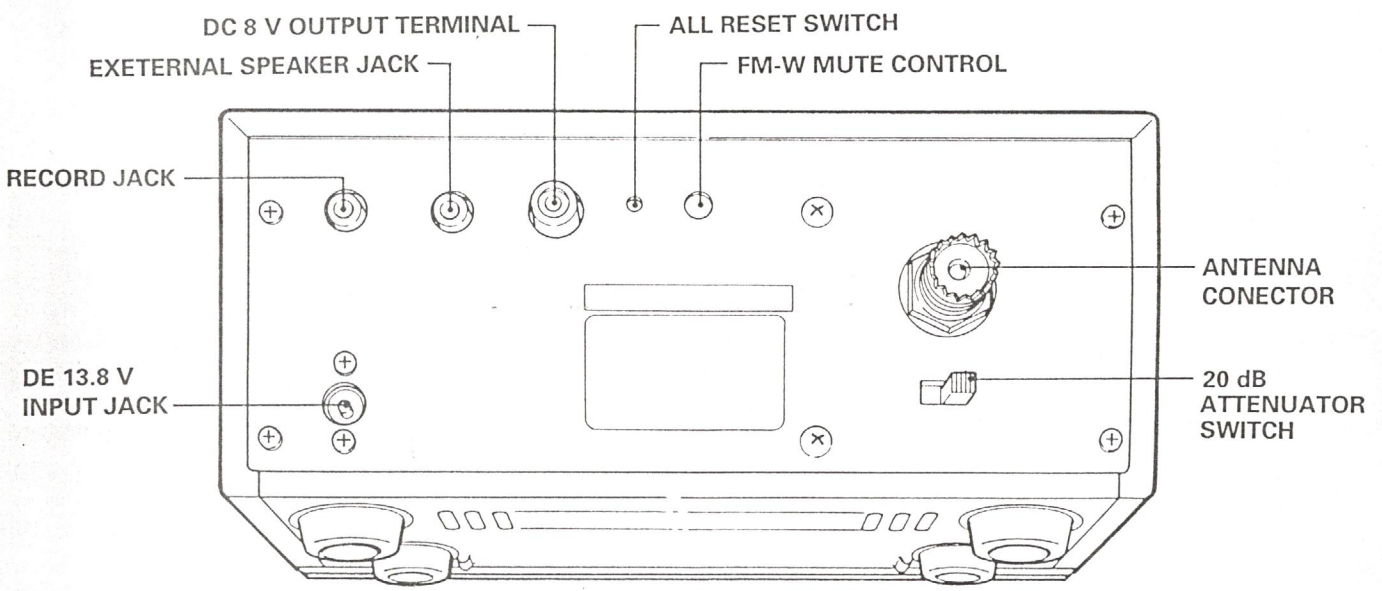
- The control and display functions of the AX700E/ES are carried out by 8-bit main and submicroprocessors.

- PLL synthesizers are used for the first IF local and second IF local circuits and the analyzer circuit.

- The tuner circuit is composed of an RF amplifier for B1 to B3, an RF amplifier for BU, a mixer, a VCO, and a first IF amplifier. The VCO generates a frequency range of 96.00 to 950.995 MHz that is 46 MHz higher than the reception frequency. Band switching between B1, B2, B3, and BU is carried out using band data and the various circuits according to the designated mode.

1. CONTROLS AND CONNECTIONS





2. MAINTENANCE

2.1 Disassembly

Before starting the adjustment procedures, be sure that the power switch of the receiver is turned off, and that the power supply and other connection cords are removed. Special care must be taken not to damage wiring or soldered parts when boards are removed.

2.1.1 Top and Bottom Covers, Rear Panel and Main Board (PM01)

a) Remove the four screws Ⓐ securing the upper cover and the five screws Ⓐ securing the bottom cover. The bottom cover can be removed by pulling it directly away from the unit. To remove the upper cover, slide it backward.
b) Remove the four screws Ⓑ and remove the rear panel.
c) Remove the four screws Ⓒ and remove the main board.

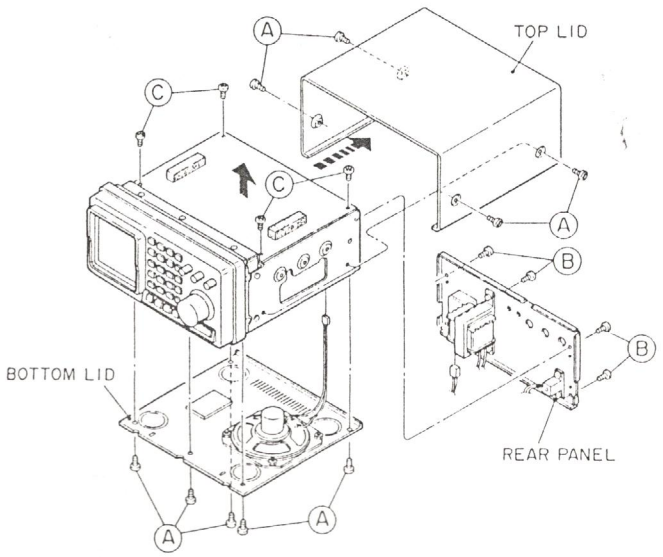


Figure 2-1

2.1.2 Sub-Control Board (PD03)

a) Remove the four screws Ⓓ and remove the front panel.
b) Remove the six screws Ⓔ. Open the shield case slightly by 2–3 cm and confirm that there are three connectors. Loosen the connectors and pull out the wiring board.
c) Remove the two screws Ⓕ and the five screws Ⓖ and remove the sub-control board.

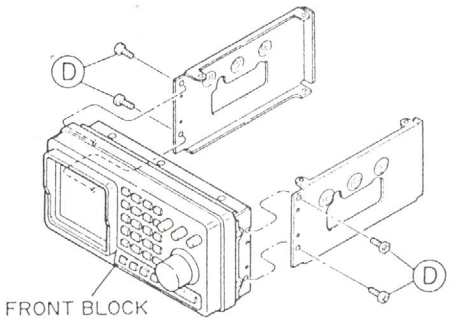


Figure 2-2

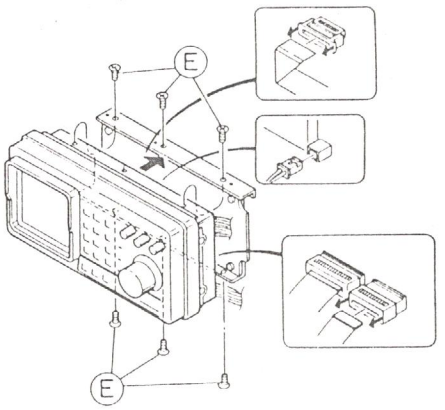


Figure 2-3

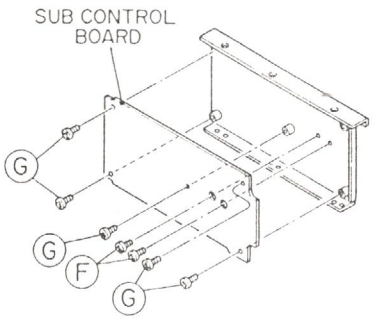


Figure 2-4

2.1.3 Main Control Board (PD01), Keyboard (PD02), and Volume Board (PM02)

a) Remove the upper and lower covers and rear panel as described in section 2.1.1 (a) and (b).
b) Remove the rotary channel selector assembly [D] and the two screws [E] and remove the front case.
c) Remove the six screws [F] and remove the main control board.
d) Remove the seven screws [G] and remove the keyboard.
e) Remove the three rubber caps [H] and the three special screws and remove the volume board.

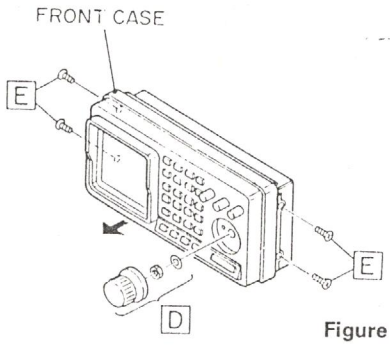


Figure 2-5

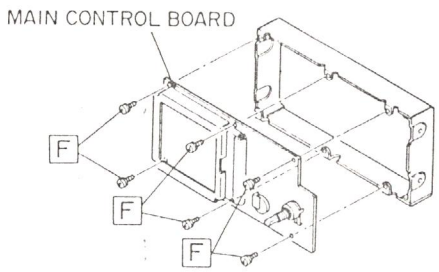


Figure 2-6

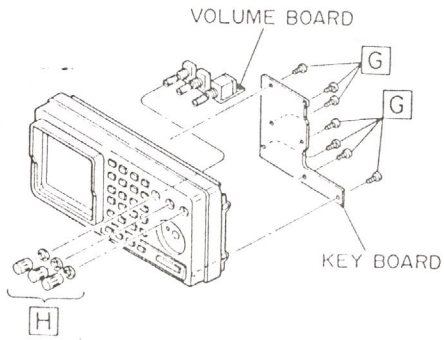


Figure 2-7

2.2 Test Set Up

For proper adjustment, the test equipment must be kept calibrated and maintained. Turn on the power supply and ensure that the test equipment is stable before starting performance test and adjustment procedures.

Conditions

Supply voltage ..... 13.8 V DC
AF dummy load 8Ω
Audio output ..... 500 mW
Adjustment frequency ..... 145.500 MHz

Standard modulation ..... FM-N ±3.5 kHz with 1 kHz
FM-W ±75.0 kHz with 1 kH
AM 30% with 1 kHz
Other conditions..... Attenuator switch OFF

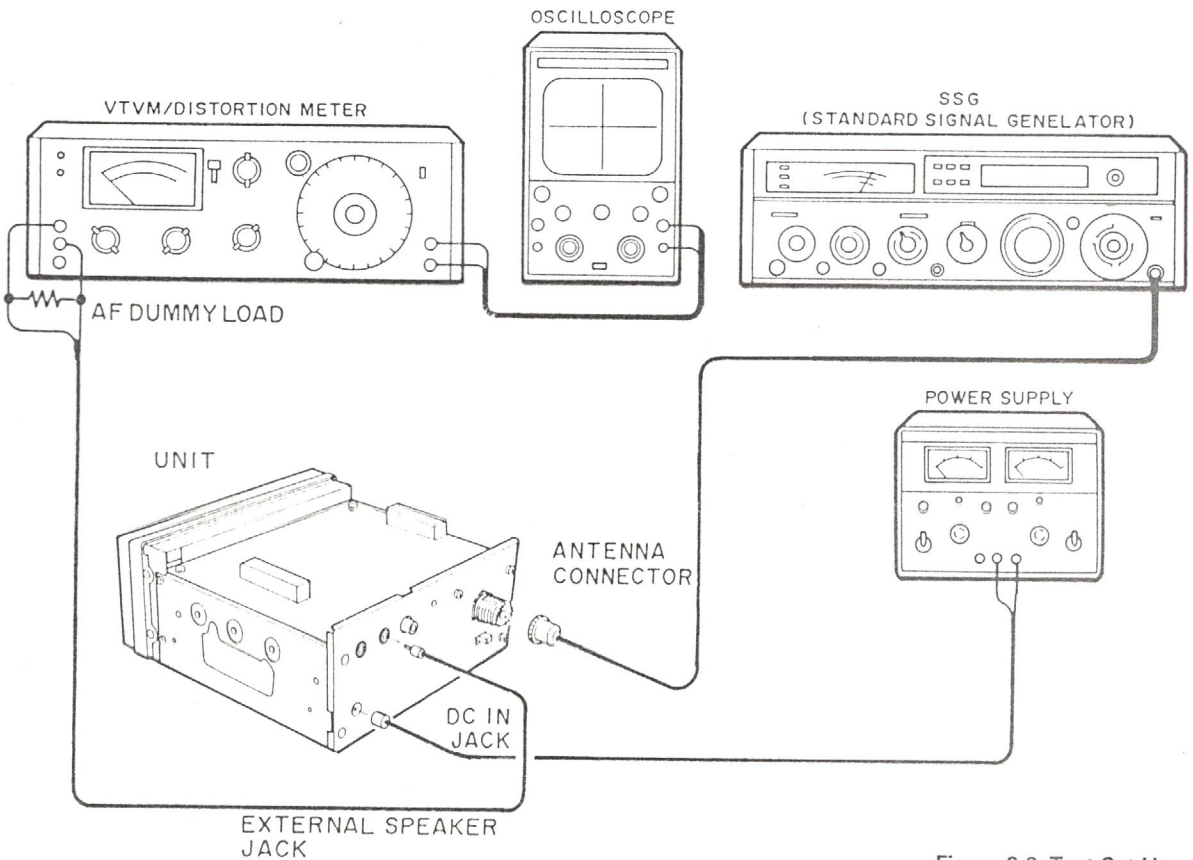
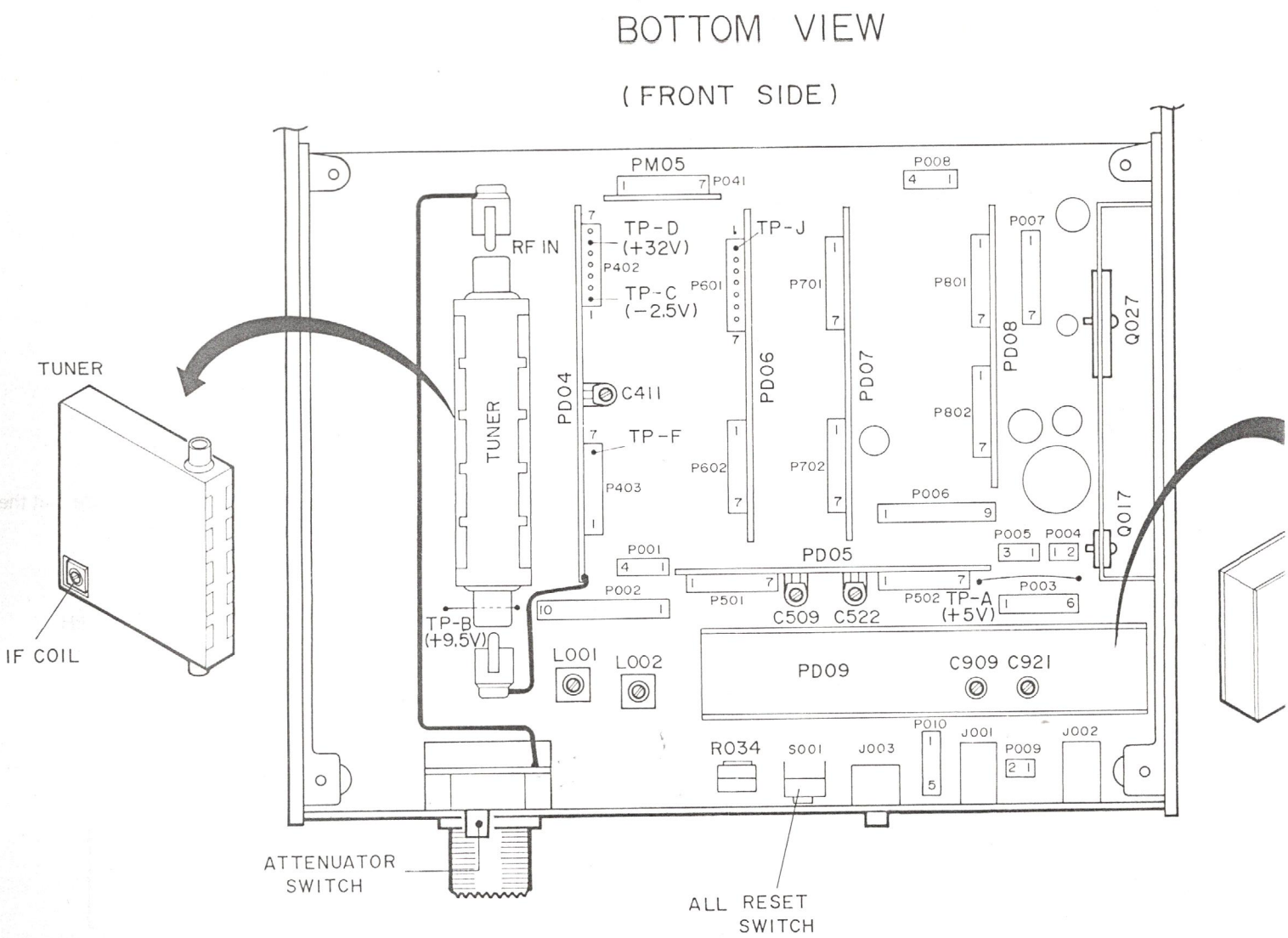
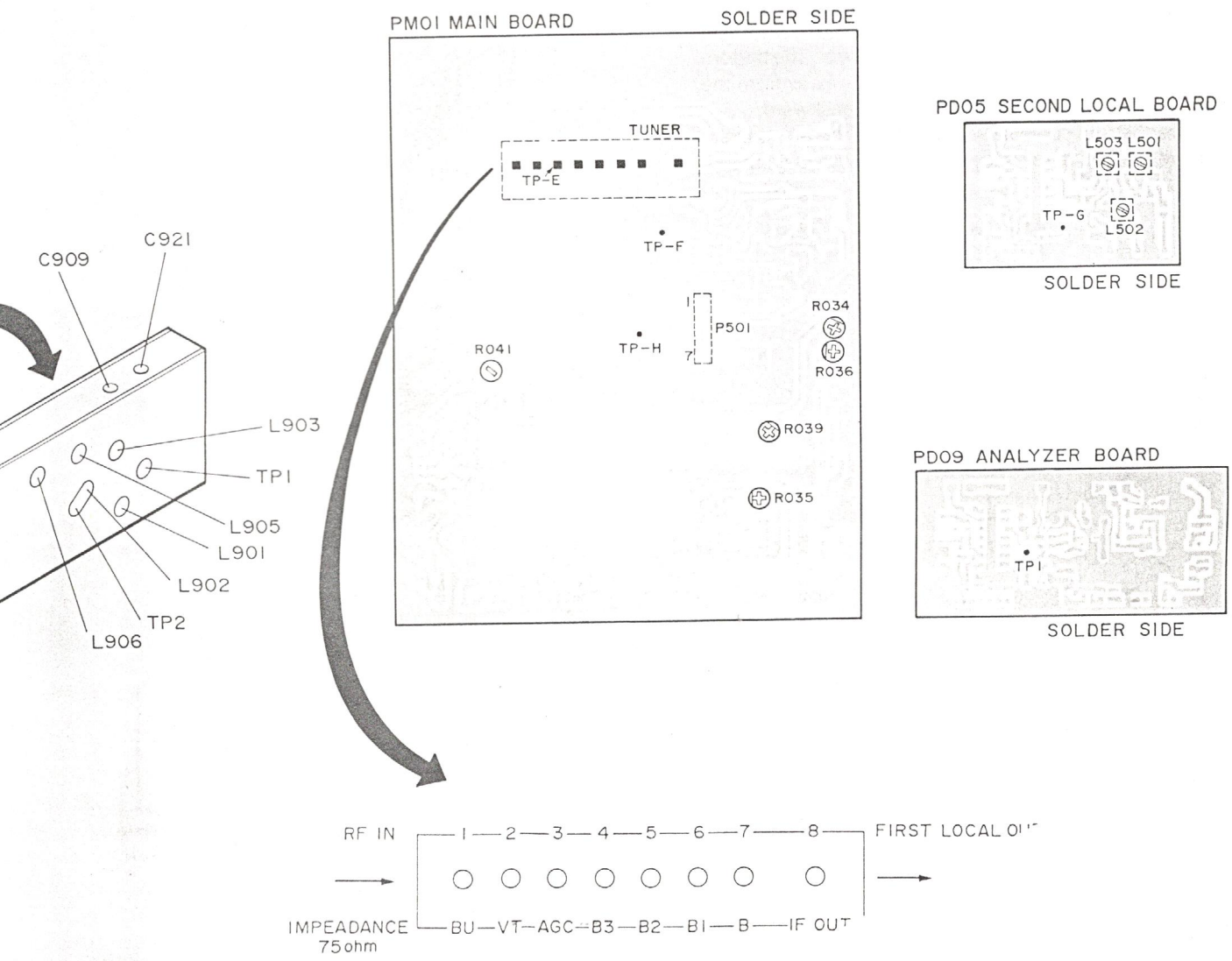


Figure 2-8 Test Set Up

2.3 Alignment Reference Points




PM01 MAIN BOARD
SOLDER SIDE
TUNER
TP-E
TP-F
TP-H
P501
R041
R034
R036
R039
R035
C909
C921
L903
TP1
L905
L901
L902
TP2
L906
PD05 SECOND LOCAL BOARD
L503 L501
TP-G
L502
SOLDER SIDE
PD09 ANALYZER BOARD
TP1
SOLDER SIDE
RF IN
1 2 3 4 5 6 7 8
FIRST LOCAL OUT
IMPEADANCE
75ohm
BU VT AGC B3 B2 B1 B IF OUT

2.4 Alignment/Performance Check

A voltmeter and frequency counter with sufficiently high impedance must be used for adjustment purposes.
Be sure to first perform the "Display Check" before proceeding to any adjustment.
After the adjustments, press the All Reset switch while the power of the unit is ON to reset the unit.

2.4.1 Display Check

a) With the All Reset switch held depressed, press the Power ON-OFF switch to ON.
b) Press the "1" key (AX700E) or "7" key (AX700ES) on the keyboard three times and check that all of the function display elements on the bandscope are lit. Otherwise, return to step a).
c) Press the Power ON-OFF switch to OFF, and proceed to the following adjustments.

2.4.2 Current Drain and Voltage Level Checks

a) Turn the Volume control of the unit to the fully counter-clockwise position.
b) Press the Power ON-OFF switch of the unit to ON, then check that the current flowing in the unit is no more than 750 mA.
c) To confirm the voltage levels, connect a voltmeter to TP-A for 4.5 to 5.5 V, TP-B for 8.5 to 10.5 V, TP-C for –3.0 to –2.0 V, and TP-D for 31.0 to 32.0 V.

2.4.3 PLL Synthesizer for First Local Circuit

Setting the VCO Frequency
a) Connect a frequency counter to TP-F (first local frequency of pin 7 of P403).
b) Set the displayed frequency of the receiver to 854.000 MHz.
c) Adjust the trimmer C411 until the frequency at TP-F falls within 900.000 MHz ±50 Hz.

2.4.4 PLL Synthesizer for Second Local Circuit

NOTE: Remove the rear panel and then the analyzer board (PD09) from the main board (PM01) before starting the adjustment of the second local circuit. After adjustment, the analyzer board must be replaced in its original position.

1) Setting the VCO Voltage
a) Pull out the core of L503 until the upper surface of the coil.
b) Connect a voltmeter to TP-G (hot side of the C525).
c) Adjust the trimmer C509 until the voltage at TP-G falls about 2.5 V.
d) Adjust L503 to maximize the voltage of C525.
e) Adjust trimmer C509 so that the voltage of C525 falls 2.5 V.

2) Setting the VCO Frequency
a) Connect a standard signal generator (SSG) to the antenna connector.
b) Set the SSG frequency to 145.500 MHz and 80 dBu without modulation.
c) Connect a frequency counter to TP-H (10.7 MHz IF at pin 4 of P501).
d) Adjust trimmer C522 until the frequency as read on the frequency counter falls within the range of 10.7000 MHz±100 Hz.
e) Connect a frequency counter to TP-J (455 kHz IF at pin 1 of P601).
f) Check that the frequency counter reads 455 kHz ±50 Hz. If the frequency counter reading is out of this range, adjust trimmer C522.

2.4.5 Sensitivity

Connect a SSG to the antenna connector.

1) General Sensitivity
a) Set the SSG frequency to 145.500 MHz±3.5 kHz deviation and modulate for a 1 kHz tone FM.
b) Set the reception frequency of the receiver to 145.500 MHz and select the AM mode by pressing the mode selection button.
c) Adjust the IF output coil of the tuner and the L001 and L002 so that the best SINAD with the maximum wave form and the minimum distortion is obtained on the oscilloscope.
d) While observing the oscilloscope, adjust L501 and L502 so that the best SINAD available (with maximized waveform and minimum distortion) is obtained.

2) Confirmation of Sensitivity for Different Modes
– FM-N Mode –
a) Set the SSG frequency to 145.500 MHz±3.5 kHz deviation and modulate for a 1 kHz tone FM.
b) Set the reception frequency of the receiver to 145.500 MHz and set to the FM-N mode by pressing the mode selection button.
c) Measure the 12 dB SINAD and confirm that the ouput level of the SSG does not exceed 0.63 μV.

– FM-W Mode –
a) Set the SSG frequency to 145.500 MHz±75 kHz deviation and modulate for 1 kHz tone FM.
b) Set the reception frequency of the receiver to 145.500 MHz and set to the FM-W mode by pressing the mode selection button.
c) Measure the 12 dB SINAD and confirm that the output level of the SSG does not exceed 1.26 μV.

– AM Mode –
a) Set the SSG frequency to 145.500 MHz and modulate for 30% AM.
b) Set the reception frequency of the receiver to 145.500 MHz and set to the AM mode by pressing the mode selection button.
c) Measure to 10 dB S/N and confirm that the output level of the SSG does not exceed 1.0 μV.

2.4.6 Bandscope: PLL Synthesizer for Analyzer Circuit

NOTE: Remove the rear panel before starting the adjustment of the analyzer circuit.

1) Setting the AM-IF Level

a) Pull out the core of L903 until the upper surface of the coil.
b) Set the SSG frequency to 145.500 MHz and 10 dBu, with 30% AM modulation.
c) Set the reception frequency to 145.500 MHz and set the Mode select button to the AM mode.
d) Connect a voltmeter to TP-E pin 3 of P053, and adjust R041 so that the voltage reading is lower by 0.4 V than the voltage when the SSG output is switched OFF.

2) Setting the VCO Voltage

a) Remove SSG from the antenna connector.
b) Set the reception frequency to 145.500 MHz and set to the FM-N mode by pressing the mode selection button. Press the bandscope display level selection button to set the scroll width of the bandscope to 100 kHz.
c) Connect a voltmeter to TP1 on the analyzer board.
d) Confirm the variation range of voltage. Adjust trimmer C909 until the center voltage is about 2.2 V.
e) Adjust L903 to maximize the voltage at TP1.
f) Adjust C909 so that the voltage at TP1 falls 2.2 V.
g) Set the SSG frequency to 145.500 MHz and 57 dBμ without modulation.
Check that the S meter display level attains the 0 V line in any mode (FM-W, FM-N, AM).
h) Set the SSG frequency to 659.000 MHz and 57 dBμ without modulation.
i) Set the displayed frequency of the unit to the same as the set frequency of the SSG. With this conditioned, check that the S meter display level attains the "S9" line in any mode (FM-W, FM-N, AM).

3) Setting the Bandscope Display Level

a) Connect a SSG to the antenna connector.
b) Set the SSG frequency to 145.500 MHz and 10 dBμ without modulation.
c) Adjust trimmer C921 for the maximum display level at a receive frequency of 145.500 MHz.
d) Adjust L902, L905, and L906 in this order for the maximum display level.
e) Set the SSG frequency to 145.500 MHz and 47 dBμ without modulation. Turn R039 to the fully counterclockwise position, and adjust resistor R035 until the display level is "0 V" (S11).
f) Set the SSG frequency to 145.500 MHz and 7 dBμ without modulation. Adjust resistor R039 until the display level is "S7".

2.4.7 Setting the Muting Level in the FM-W Mode

a) Set the SSG frequency to 50.000 MHz and –1 dBμ, with 1 kHz ±75 kHz tone FM modulation.
b) Set the displayed frequency of the unit to 50.000 MHz, and set the Mode select button to the FM-W mode.
c) Turn R034 to the fully clockwise position, and adjust R036 so that the monitored sound can be heard from the speaker.
d) Set the SSG frequency to 50.000 MHz and –3 dBμ, with 1 kHz ±75 kHz tone FM modulation. With this condition, check that the monitored sound is not heard from the speaker.
e) Set the SSG frequency to 50.000 MHz and 1 dBμ, with 1 kHz ±75 kHz tone FM modulation. With this condition, check that the monitored sound is heard from the speaker.
f) Set the SSG frequency to 94.000 MHz and –3 dBμ, with 1 kHz ±75 kHz tone FM modulation.
g) Set the displayed frequency of the unit to the same as the set frequency of the SSG, and set the Mode select button to the FM-W mode. With this condition, check that the monitored sound is not heard from the speaker.
h) Set the SSG frequency to 94.000 MHz and 1 dBμ, with 1 kHz ±75 kHz tone FM modulation. With this condition, check that the montored sound is heard from the speaker.
i) Set the SSG frequency to 145.000 MHz and –3 dBμ, with 1 kHz ±75 kHz tone FM modulation.
j) Set the displayed frequency of the unit to the same as the set frequency of the SSG. With this condition, check that the monitored sound is not heard from the speaker.
k) Set the SSG frequency to 145.000 MHz and 1 dBμ, with 1 kHz ±75 kHz tone FM modulation.
l) Set the displayed frequency of the unit to the same as the set frequency of the SSG, and set the Mode select button to the FM-W mode. With this condition, check that the monitored sound is heard from the speaker.

A 2

3. SPECIFICATIONS

Frequency Range	50.000 to 904.995 MHz (Specification gurantee range for Model AX700E) 144.000 to 145.995 MHz 430.000 to 439.995 MHz (Specification gurantee range for Model AX700ES) 50.000 to 904.995 MHz (Range indicated in LCD display for Model AX700ES)
Antenna Impedance	50 Ω
Frequency Step	10, 12.5, 20, and 25 kHz (AJ MODE 5 kHz, UP/DOWN BUTTON 1 kHz)
Number of Memory Channels	100 channels
Number of Program Search Memory Bands	10 bands
Sensitivity	AM (10 dB SINAD): 3 μV or less FM-N (12 dB SINAD): 1.5 μV or less FM-W (12 dB SINAD): 1 μV or less at 83 MHz
Squelch Sensitivity (FM-N Mode)	0.2 μV or less
Audio Power Output	External Speaker Terminal: 1.8 W or more, 8 Ω, 10% distortion, Input signal of FM 1 kHz±3.5 DEV Recorder Terminal: 30 mW (load of 100 kΩ)
8 V Output Terminal	8 V 40 mA maximum
Power Supply	DC 13.8 V±15%
Current Drain	1 A (audio output 2 W)
Ground	Negative Grounding
Operating Temperature Range	0 – 50°C
Dimensions	75-H x 180-W x 180-D mm (excluding projections)
Weight	2.1 kg (including the antenna stand)

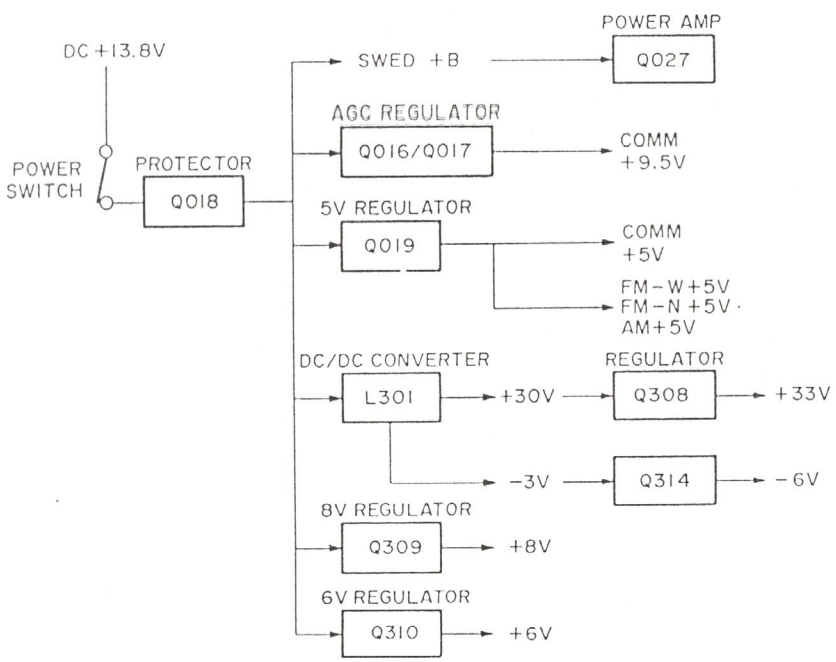
Performance specifications are nominal, Unless otherwise indicated, and are subject to change without notice.

4. THEORY OF OPERATION

4.1 Power Supply Circuitry

The following voltage levels are used for the AX700E/ES:

Table 4-1 Voltage



4.2 Front End: Tuner Circuit (RF Amplifier/First Mixer/First IF Amplifier)

The signal picked up by the rod antenna is passed through the 20 dB attenuator circuit (R051 and R052), and applied to the RF input terminal of the tuner circuit P053. The tuner circuit contains an RF amplifier for the B1–3 and BU bands, mixer, VCO, and first IF amplifier. The VCO generates the first local frequency of 96.00–950.995 MHz, which is 46 MHz higher than the incoming signal, over all the bands. The signal input to the tuner circuit is amplified by the RF amplifier and passed through the mixer and IF amplifier. This signal comes out of the IF output terminal and is converted to the 46 MHz first IF signal. The 46 MHz first IF signal is passed through the diode IF switch Q001, analyzer circuit, Q001 buffer Q005, and band switching circuit Q006–Q009, after which the signal is applied to the second IF circuit.

B1, B2, B3, and BU on the tuner are bias terminals for their corresponding bands. These bands are controlled by applying band data from the main microprocessor Q101 to pins 1 and 2 of band selector Q407 and controlling Q407 output terminal pins 12–15. Pins 12–15 are connected to the two-stage band switch, after which they are connected to the bias terminal for each band. Bias voltage is +9.5 V. Voltage of +0.5 to +9.5 V is applied to the VT terminal for each band to control the frequency (first local frequency) of the VCO located inside the tuner.

The first local frequency is output from the first local output terminal, passed through amplifier Q416 and Q401, and applied to the PLL prescaler for the first local Q402.

Band Selector Q407 Function List Table 4-2

Pin No.	Input		Output			
	1	2	15	14	13	12
Level	L	L	H	L	L	L
	H	L	L	H	L	L
	L	H	L	L	H	L
	H	H	L	L	L	H

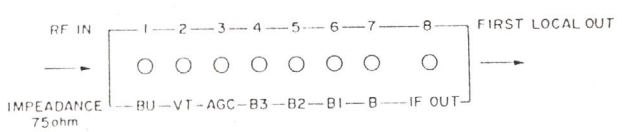


Figure 4-1 Tuner Jack (P053)

4.3 Analyzer Circuit

The analyzer circuit is designed to convert the incoming signal to DC voltage to pick up the level detection output. This output is converted to a digital signal by the A/D converter Q302, and displayed as a spectrum level on the bandscope by common and column drivers Q107–Q109.
The 46 MHz first IF signal is passed through the diode IF switch Q001, after which the input level is adjusted by resistor R037, and the signal is applied to pin 1 of the second IF IC Q901 of the analyzer, circuit. Q901 is composed of an amplifier, mixer and VCO. Pin 6 outputs the 10.7 MHz second IF signal. This signal is passed through the crystal filter F901, applied to the third mixer Q907, and heterodyned with the 10.245 MHz signal on the third local oscillator. The 455 kHz third IF signal created by Q907 is passed through the tuning circuit L906 and ceramic filter F902, and applied to pin 1 of IF IC Q909. Q909 contains an amplifier and detector, and outputs the level detection signal to pin 3. The level detection output in proportion to the field strength of the incoming signal is adjusted for the display level by resistor R035 on the rear panel, and applied to pin 2 of the A/D converter Q302 of the sub-controller. Q302 outputs the detection signal, which was converted to a digital signal, from pins 4–9, 11, and 12 to the sub-microprocessor Q301. The digital signal is displayed on the LCD through the common driver Q107 and column drivers Q108 and Q109.

4.4 Second IF Circuit: Band Switching Circuit

The 46 MHz first IF signal is passed through the diode IF switch Q001 buffer Q005, and applied to band switching circuits Q006 and Q008 or Q007 and Q009 by setting the receiver to the desired mode. When the receiver is set to the FM-N or AM mode, band switching circuits Q006 and Q008 are forward biased. The 46 MHz IF signal is passed through the band pass filter F001 and coupled with pin 1 of the second IF IC Q501.
When the receiver is set to the FM-W mode, band switching circuits Q007 and Q009 are forward biased, and the 46 MHz IF signal is coupled with pin 1 of Q501.

Q501 contains an amplifier, mixer, and VCO. Pin 6 outputs the 10.7 MHz second IF signal. The VCO output frequency of pin 7 of Q501 is applied to pin 3 of the PLL IC Q503.

4.5 Third IF Circuit and Detector Circuit

The 10.7 MHz second IF signal on pin 6 of Q501 is passed through the IFT L502, and applied to the detector circuit Q702 for FM-W/AM modes and the third IF circuit Q602.

- FM-W mode
  The second IF signal is detected by the detector circuit Q702 for FM-W and AM modes to obtain a voice signal.
- FM-N mode
  The second IF signal is converted to 455 kHz by the third IF circuit Q602 and detected to obtain a voice signal.
- AM mode
  The second IF signal is converted to 455 kHz by the third IF circuit Q602, and input to and detected by the detector circuit Q702 for FM-W and AM modes to obtain a voice signal.

4.5.1 FM-W Mode

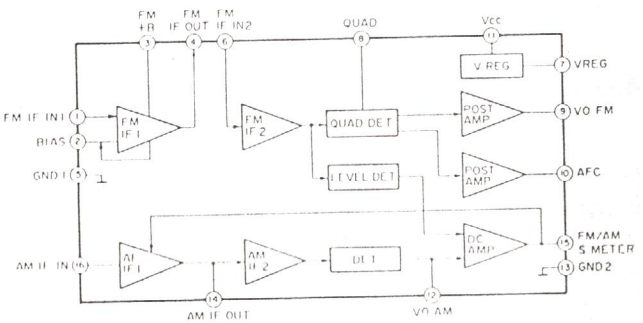


Figure 4-2 FM/AM IC Q702

In FM-W mode, the second IF signal is passed through the IF amplifier Q701 and crystal filter F701 and applied to pin 1 of the FM IF input terminal of detector circuit Q702 for FM-W/AM modes. This signal is then passed through the internal amplifier, the crystal filter F703, which has been connected externally to pins 4 and 6, the quadrature detector, and the amplifier. The FM-W detection signal is output to pin 9.
The 455 kHz third IF signal, which passed the band pass filter F703, is applied from pin 5 of the third IF circuit Q602 to Q702 AM IF input terminal pin 16. During the FM-W mode, the 455 kHz third IF signal is not input to Q702 AM IF input terminal pin 16 because of FM-W +5 V being supplied to the base of the AM IF switch Q703, which creates ground potential.

4.5.2 FM-N/AM Modes

In FM-N mode, the 10.7 MHz second IF signal is passed through the buffer amplifier Q601 and a pair of crystal filters F601 and input to pin 16 of the third IF circuit Q602. Q602 contains an amplifier, mixer, 10.245 MHz local oscillator, limiter circuit, detector circuit, and peripheral circuits. the FM-N detection signal is output from pin 9 of Q602. This signal is passed through the de-emphasis circuit R610, C613, R611, and C624, and applied to the audio signal switching circuit. Part of the 455 kHz third IF signal on pin 5 is passed through the buffer amplifier Q606 and band pass filter F703 and input to AM IF input terminal pin 16 of detector circuit Q702 for FM/AM modes.
In AM mode, AM +5 V is applied to the buffer amplifiers. Q601 and Q606 and the 455 kHz third IF signal is input to AM IF input terminal pin 16 of detector circuit Q702. This signal is passed through the second stage of the internal amplifier and AM detector, which outputs the AM detection signal to pin 12. The AM detection signal is passed through the de-emphasis circuit R711 and C720 and applied to the audio signal switching circuit Q801–Q807.

4.6 Automatic Gain Control (AGC) Circuitry

In tghe FM-W/AM modes, the AGC circuit serves to optimize the detected output of pin 15 of the FM-W/AM mode detector circuit Q702. The AGC circuit is composed of diode Q051 and transistors Q052, Q010, Q012, and Q704. The detection output of pin 15 of Q702 is appled to Q704. The Q010 base, Q011 collector, and Q012 base are connected to the Q704 emitter.
SWED+B is a constant voltage circuit consisting of Q016 and Q017 and stabilized at +9.5 V. a voltage of +9.5 V is divided into +6.5 V by resistors R017 and R018 of the AGC circuit. This reference voltage of +6.5 V is applied to the AGC circuit Q012 collector, pin 3 AGC terminal of the tuner circuit P053, and the amplifier Q052 base.
The detected output of pin 15 of Q702 is in proportion to the intensity of the incoming signal. The reference voltage of +6.5 V is reduced through Q012 until the detected voltage of pin 15 of Q702 is optimized.

4.7 Audio Signal Switching Circuit

The audio signal switching circuit applies mode data on pin 13 of the interface Q102 (AM), pin 14 (FM-N), and pin 15 (FM-W) to the base of the DC switch Q022 for the AM mode, Q021 for the FM-N mode, and Q020 for the FM-W mode, and is switched among these modes according to the mode selected on the receiver. Table 4-3 shows the active circuits for different modes. The voice signal passed through the audio signal switching circuit is applied to the audio scanning circuit Q808 and mute circuits Q805 and Q807.

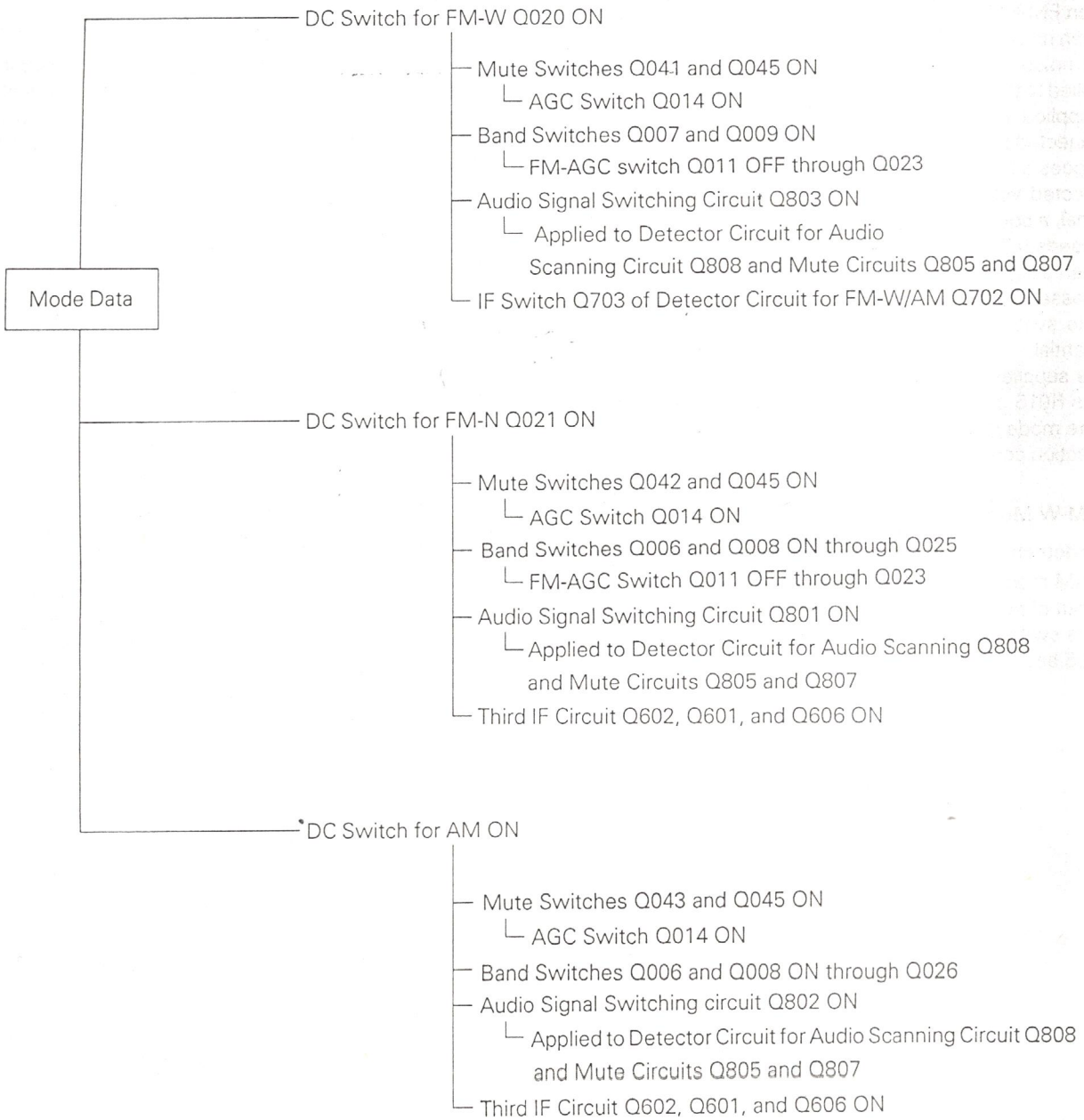
4.7.1 Detector Circuit for Audio Scanning

When the audio scan mode (AF.SCAN) is selected from the various scan modes, the voice signal input to the detector circuit for audio scanning is passed through the amplifier Q808. This signal is converted to DC voltage by the voltage doubler rectifier Q809 and Q810 and applied to the switch Q811. Q811 goes "low" when a voice signal is present. This Q811 collector output is fed to pin 63 of the main microprocessor Q101 and acts as a control signal for audio scanning. When pin 63 of Q101 is low, the PLL circuit is controlled to stop scanning temporarily. When pin 63 goes high, scanning is resumed.

4.7.2 Mute Circuit Operation Chart for Different Modes

The following chart shows the activation of mute circuits for different modes:

Table 4-3 Active Circuits for Different Modes



4.7.3 Audio Mute Circuit and Squelch Circuit

When no signal is being received in any of the FM-W, FM-N, and AM modes, a voice signal in these modes is muted because of reverse biased mute switch Q014 that controls audio mute circuits R816, R815, and Q805, R819, R818, and Q806.

– FM-N/AM Modes –

A squelch signal on pin 13 of the third IF circuit Q602 is used as an FM-N/AM mute signal.
When no signal is being received in FM-N or AM mode, the 30 kHz noise component passed through the noise amplifier is applied to the noise detector, after which the detected voltage is applied to pin 12. The internal squelch switch of Q602 connected to pin 12 is activated so that a squelch signal on pin 13 goes a logic "high" or "low", depending on the level of this detected voltage, in reference to 0.7 V. When there is no signal, a squelch signal on pin 13 goes "low", because pin 12 exceeds 0.7 V.
When a signal is being received, a logic "high" squelch signal is passed through the diode switch Q603 and applied to the mute switch Q014 base. The Q014 collector goes ground potential.
This supplies current to the audio mute circuit through the lines R015 and R017 connected to the collector. The audio mute mode is cleared and a voice signal that matches mode selection conditions is applied to the audio amplifier Q027.

– FM-W Mode –

The detected output of pin 15 of the detector circuit for the FM-W/AM modes is used as a FM-W mute signal. The detected output of pin 15 of Q702 is input to the AGC circuit Q704 and mute switch Q705. R034 is adjusted until the voltage at the Q705 base optimizes the muting level.

When a signal is being received, the mute switch Q705 collector goes ground potential and the next stage mute switch for the FM-W mode Q804 is reverse biased. A voltage of FM-W +5 V is applied to the Q804 collector. This voltage forward biases the diode switch Q806 and mute switch Q014. This forms ground potential at the Q804 collector. The audio mute mode is cleared as with the "FM-N/AM modes", and the FM-W mode voice signal is applied to the audio amplifier Q027.

4.7.4 Mode Voltage Mute Circuit

This circuit removes changes in DC which may occur when the mode is switched and would cause noise being heard from the speaker. The mode voltage of each mode – FM-W +5 V, FM-N +5 V, and AM +5 V – is applied to each of the mode voltage mute circuit Q041–Q044 with time constants provides by C041–C044. The "high" FM-W, FM-N/AM mute signal is applied to the switch Q045 collector, based on which Q045 is forward biased. The switch Q045 grounds surge voltage caused by switching the mode.

4.8 PLL Synthesizer

The AX700E/ES uses PLL synthesizers for the first and second local and analyzer circuits. PLL synthesizers used for the second local and analyzer circuits have a similar circuit structure.

4.8.1 First Local Circuit

– Block Diagram of PLL at 10 kHz Channel Step –

The PLL IC Q404 is composed of a reference divider (1/R), phase comparator (P/C), and programmable divider (1/N). VCO is incorporated into the tuner. VCO frequency is 96.00–950.995 MHz that is 46 MHz higher than that of the incoming signal. Division ratios 1/R and 1/N are determined by PLL serial data.

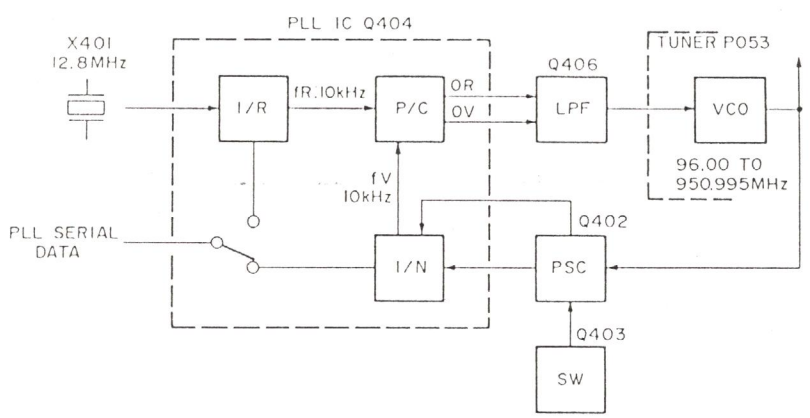


Figure 4-3 PLL Block Diagram

– Equation for Calculating the N Number –

$$N = \frac{\text{Reception frequency + First IF (46)}}{\text{Channel step (0.01)}} \text{[MHz]}$$

Relationship Between fR/fV and OR/OV Table 4-4

fR/fV Combination	Output	
	OV	OR
Leading fV>fR	Lo	Hi
Lagging fV>fR	Hi	Lo
Lock fV=fR	Hi	Hi

– Reference Frequency (fR) –

The 12.8 MHz crystal resonator X401 is used for the reference oscillator. An oscillator frequency of 12.8 MHz is divided to a reference frequency of 10 or 12.5 MHz by the reference divider.
There are four channel steps: 10, 12.5, 20, and 25 kHz. When the channel step is at 10 or 20 kHz, the reference frequency goes to 10 kHz. When the channel step is at 12.5 or 25 kHz, the reference frequency goes to 12.5 kHz.

– Programmable Divider –

The programmable divider and prescaler (PSC) Q402 form a pulse swallow counter.
Switch Q403 switches prescaler pin 6 to "high" or "low" according to the control signal from pin 25 of main microprocessor Q101. The prescaler is 1/64 when pin 6 is "high", and 1/128 when it is "low". The VCO oscillation frequency in the range of 96.00 to 950.995 MHz is processed by the prescaler and programmable divider to become the comparison frequency (fV) of 10 or 12.5 kHz.

– Phase Comparator/Low Pass Filter –

The phase comparator compares the phase of fR from the reference divider with that of fV from the programmable divider. Phase comparison output is output to pins 15 (OV) and 16 (OR) and applied to the low pass filter Q406 (1/2). The differential low pass filter converts the OR-OV relation to the shift voltage that is applied to VCO and determines the direction in which the VCO frequency shifts.

– Unlock Signal –

The lock detection output of pin 7 of PLL IC Q404 goes "low" when PLL is unlocked (asynchronous).

4.8.2 Second Local Circuit/Analyzer Circuit

1) Second Local Circuit

– Block Diagram of PLL at 1-kHz Channel Step –

PLL IC Q503 is composed of a reference divider (1/R), phase comparator (P/C), and programmable divider (1/N). The second IF IC Q501 VCO is used. VCO frequency is 35.3±0.005 MHz that is 10.7 MHz lower than that of the incoming signal. Division ratios 1/R and 1/N are determined by PLL serial data.

The PLL circuit for the second local circuit always obtains a second IF frequency of 10.7 MHz in concert with the PLL circuit for the first local circuit.

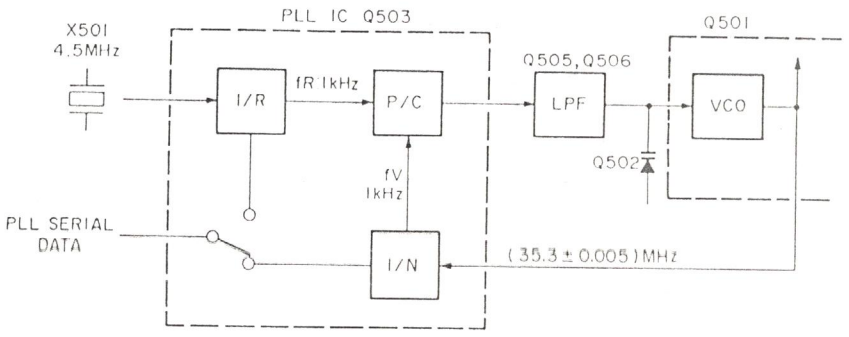


Figure 4-4 PLL Block Diagram

– Equation for Calculating the N Number –

$$N = \frac{\{\text{First IF frequency } (46 \pm 0.005) - \text{Second IF frequency } (10.7)\}}{\text{Channel step } (0.001)} \text{ [MHz]}$$

– Reference Frequency (1/R) –

The 4.5 MHz crystal resonator X501 is used for a reference oscillator, and its frequency is divided into a reference frequency of 1 kHz by the reference divider built into the PLL IC Q503.

– Programmable Divider (1/N) –

A VCO frequency of 35.3±0.005 MHz is passed through the programmable divider and converted to a comparison frequency of 1 kHz.

– Phase Comparator (P/C) –

The phase comparator compares the phase of a reference frequency of 1 kHz with that of a comparison frequency of 1 kHz. The output pin 10 of the phase comparator generates the following three output signals at the phase of signal 2:

- Advanced phase ..... "High"
- Delayed phase ..... "Low"
- Lock (synchronous) ..... High impedance

– Unlock Signal –

The lock detection output of pin 11 of PLL IC Q503 goes "high" when PLL is locked. It goes "low" when PLL is unlocked.

– Low Pass Filter –

The phase detection output of pin 10 is converted to DC current (shift voltage) by the PLL loop filter Q505 and Q506. The shift voltage is applied to the variable capacitor diode Q502 and then pin 8 of Q501 and controls the frequency of the internal VCO of Q501.

– VCO –

The VCO generates a frequency of 35.3±0.005 MHz that is 10.7 MHz lower than the first IF frequency.

2) Analyzer Circuit

The reference frequency goes to 10 kHz when the channel step is 10 or 20 kHz and 12.5 kHz when the channel step is 12.5 or 25 kHz.
When a bandscope display level of 1 MHz is selected, the VCO frequency is 35.3±0.5 MHz. In this case, the main microprocessor activates the analyzer circuit PLL circuit for scanning the frequency of the microprocessor clock at a channel step of 10 or 12.5 kHz in reference to 35.3 MHz.

4.9 Controll

The functions of the I/O port are summarized in the table given below.

4.9.1 Main Microprocessor Q101

Table 4-5

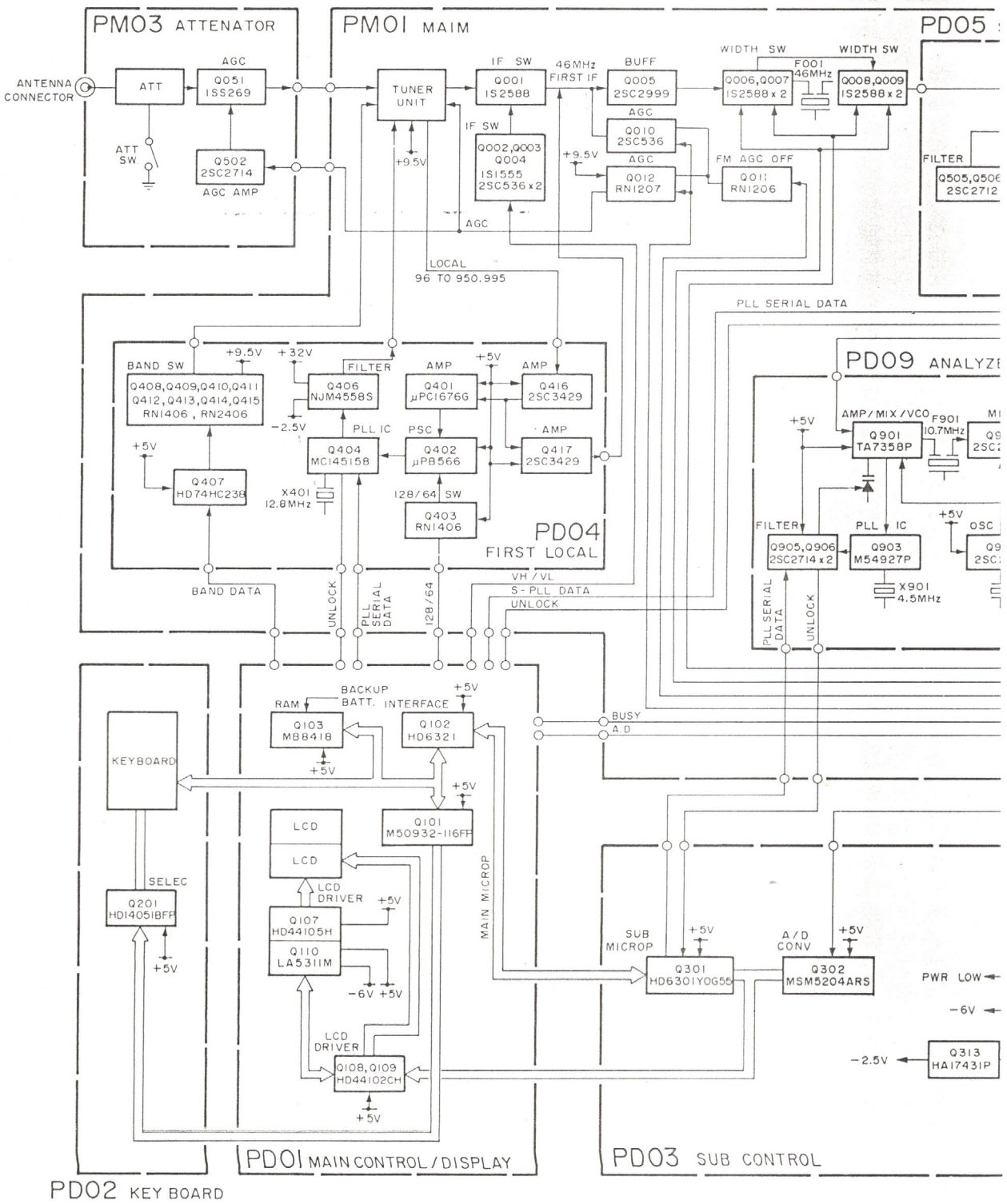
Pin No.	I/O	Symbol	Description
1~9	O	SEGMENT 8~0	LCD segment terminal
10~13	O	COMMON 3~0	LCD common terminal
14~16	I	VL1~VL3	Vcc is divided by R109~R112. LCD contrast that provides a reference voltage for the LCD bias is adjusted by R112.
17	–	Vcc	(+5±0.5)V DC
18	O	BUZZER	Rectangular output is rectified for waveform and adjusted for level.
19	O	PLL ENABLE	With this pin, "high" indicates that data transmission to the PLL for the first/second local circuits is completed.
20	O	PLL CLOCK	Synchronous clock for PLL for the first/second local circuits.
21	O	PLL DATA	Data to be sent to PLL for the first/second local circuits.
22	O	$\overline{\text{MUTE}}$	When this pin goes "low", it acts as a test terminal (unused).
23	O	PLL SELECT	When this pin goes "low", PLL serves for the first local circuit. When this pin goes "high", PLL serves for the second local circuit.
24	I	$\overline{\text{ROT CH SELE CLK}}$	This pin is inputted when the "low" rotary channel selector is rotated.
25	O	128/$\overline{64}$	"Low/high" reception frequency is output to the PLL for the first local circuit.
26	O	$\overline{\text{RESET}}$	When this pin goes "low", the detected low voltage is output and all ICs are reset.
27	I	$\overline{\text{POWER LOW}}$	When Vcc falls to +4.5 V in the voltage detector circuit (Q305–Q307), this pin goes "low".
28	–	Vss	Ground
29	I	$\overline{\text{RESET}}$	Resets Q101 while the delay circuit C102, Q116, and R106 keeps the microprocessor "low" for more than 10 msec after turning on the power switch.
30	I	X IN	Clock input terminal (frequency: 4.0 MHz)
31	O	X OUT	Clock output terminal (frequency: 4.0 MHz)
32	–	Vss	Ground.
33~40	I/O	MAIN DATA 7~0	NOTE 1
41	O	READ/$\overline{\text{WRITE}}$	When this pin goes "low", data is written to Q102 or Q103. When this pin goes "high", data is read from Q102 or Q103.
42	O	PIO E	Synchronous signal for writing data to Q102 or reading data from Q102.
43	O	$\overline{\text{RAM CS}}$	When this pin is "low", data is read from RAM Q103.
44	O	$\overline{\text{PIO CS}}$	When this pin is "low", data is read from PIO Q102.
45	O	$\overline{\text{KEY READ}}$	When this pin is "low", a signal from the keyboard is read.
46~53	O	ADDRESS 10~3	Addressing signal for writing data to Q103 or reading data from Q103.
54~56	O	ADDRESS 2~0	Output data for key scan to Q201 (NOTE 2).
57	I	$\overline{\text{CONV. SENSI.}}$	Present when converter is "Lo", not present when converter is "Hi".
58	I	$\overline{\text{ALL RESET}}$	When the ALL RESET key is pressed, this pin goes "low". When the key is not pressed, this pin goes "high".
59	I	$\overline{\text{ACK}}$	When a command from Q301 and Q101 is read, this pin goes "low".
60	I	CW/$\overline{\text{CCW}}$	When the rotary channel selector is rotated counterclockwise, this pin goes "low". When the selector is rotated clockwise, this pin goes "high".
61	I	$\overline{\text{SECOND PLL UNLOCK}}$	When PLL for the second local circuit is unlocked, this pin goes "low". When the PLL is locked, this pin goes "high".
62	I	$\overline{\text{FIRST PLL UNLOCK}}$	When PLL for the second local circuit is unlocked, this pin goes "low". When the PLL is locked, this pin goes "high".
63	I	AF SCAN	When no voice signal is not being received, this pin goes "low". When a voice signal is being received, this pin goes "high".
64	I	$\overline{\text{SQUELCH}}$	When the squelch circuit is activated, this pin goes "low". When the squelch circuit is inactive, this pin goes "high".
65~72	O	SEGMENT 23~16	For column drivers.
73	–	Vss	Ground.
74	–	SEGMENT 15	Unused.
75~80	O	SEGMENT 14~9	For column drivers.

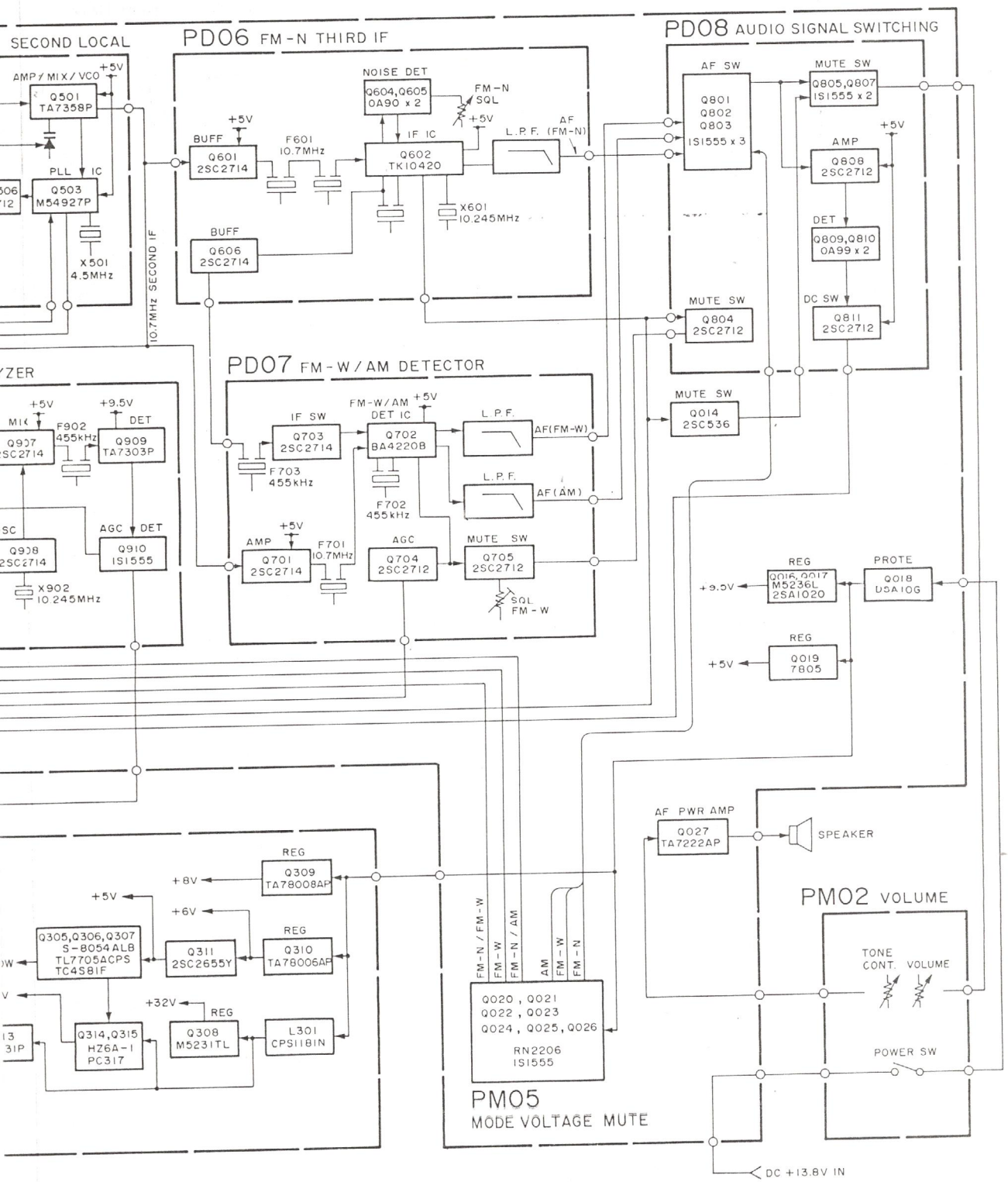
4.9.2 Submicroprocessor Q301

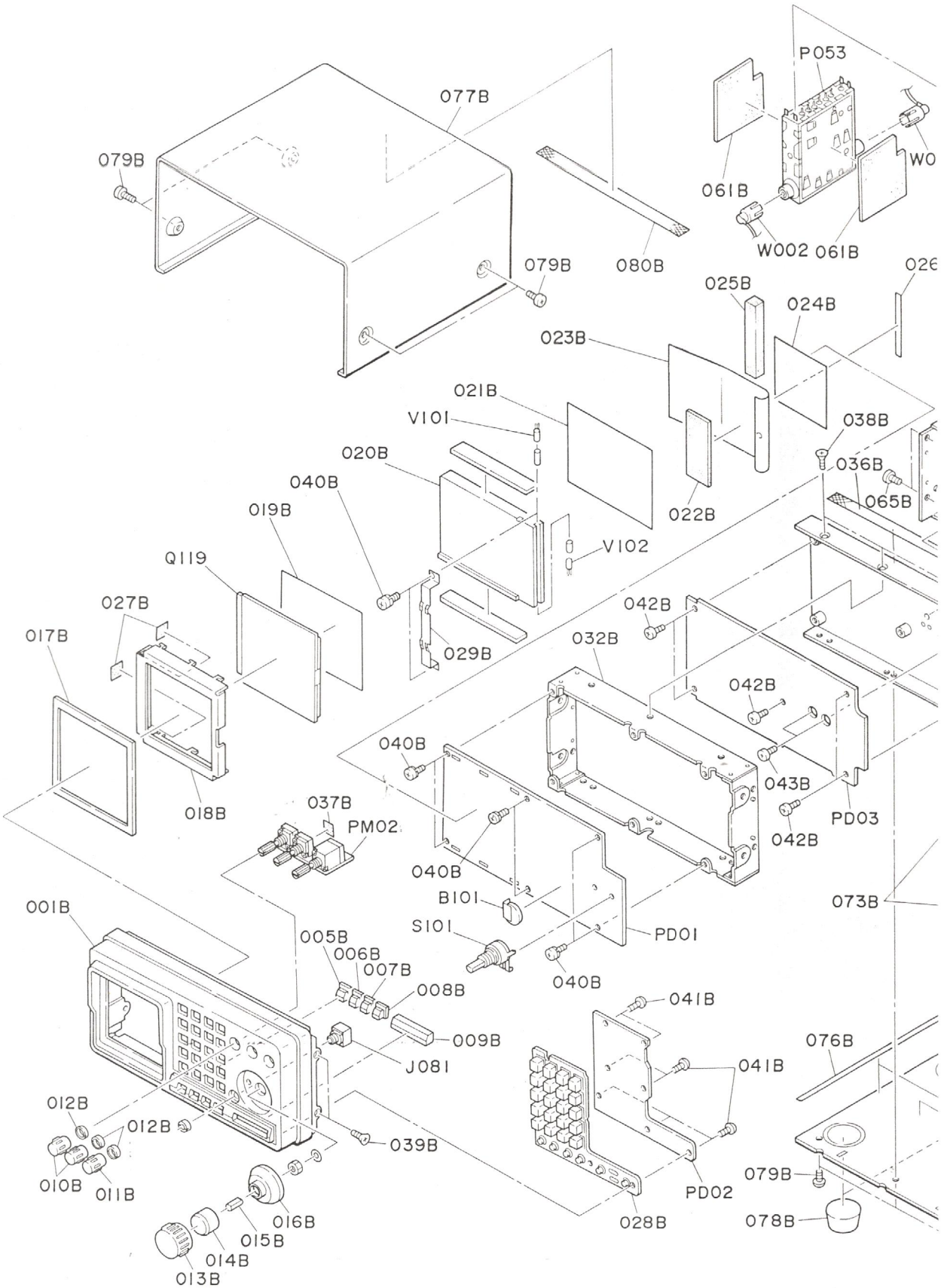
Table 4-6

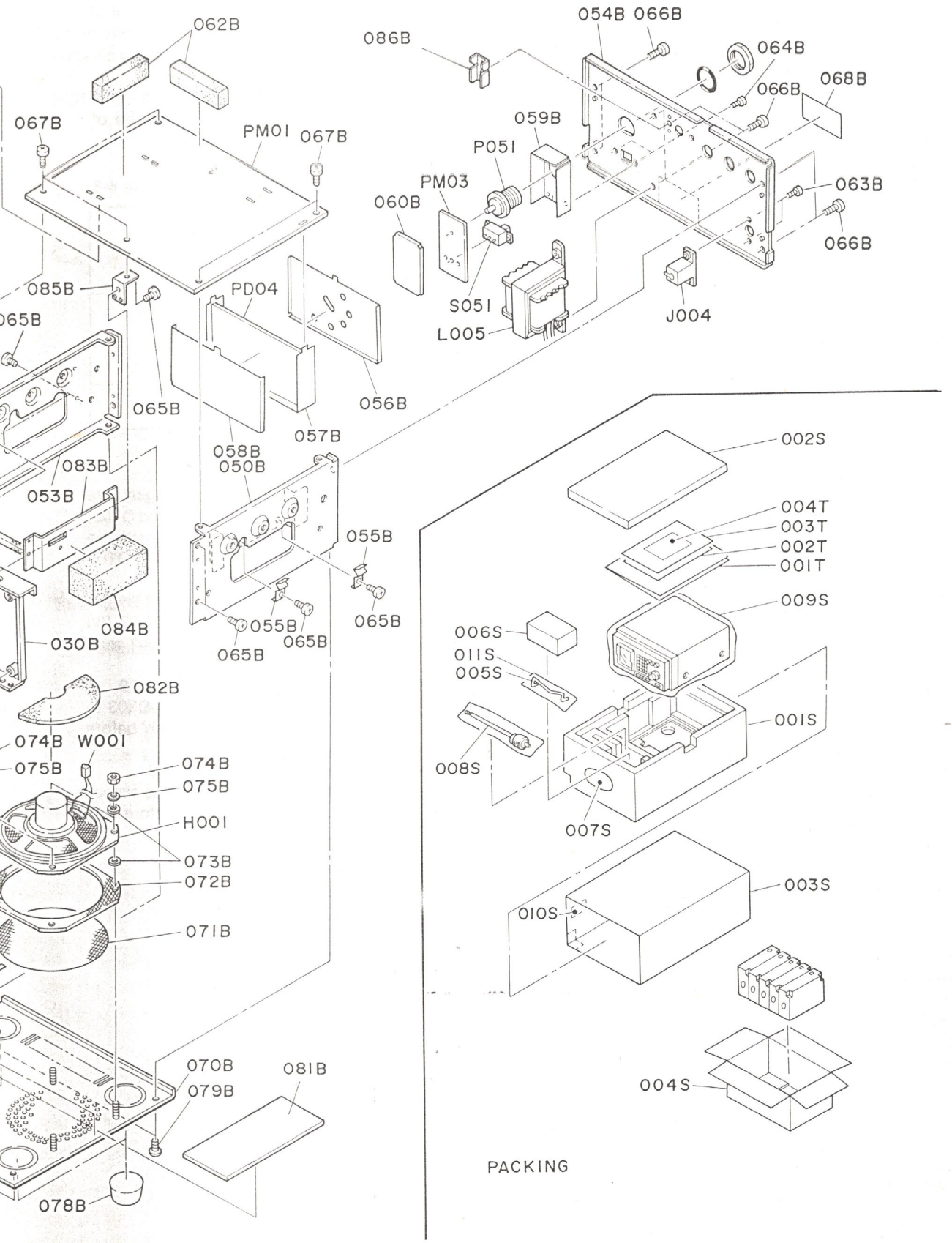
Pin No.	I/O	Symbol	Description
1	O	Vss	Ground.
2	O	X OUT	Clock output terminal (frequency: 4.0 MHz)
3	I	X IN	Clock input terminal (frequency: 4.0 MHz)
4, 5	I	MP 0, MP 1	When connected to VCC and Q301 is set to the single chip mode, these pins go "high".
6	I	$\overline{\text{RESET}}$	Resets Q301 while the delay circuit C102, Q116, and R106 keeps the microprocessor "low" for more than 10 msec after the power switch is turned on.
7	I	STANDBY	Unused. Connected to Vcc to keep the high status.
8	I	$\overline{\text{NMI}}$	Unused. Connected to Vcc to keep the high status.
9	O	$\overline{\text{ACK}}$	When Q101 completes reading command from Q301, this pin goes "low".
10	O	P21	Unconnected.
11	O	ANALYZER PLL CLK	Synchronous clock for analyzer PLL (Q304 reverses the high and low states of the clock; pin 4 of J303 outputs clock.)
12	O	ANA. PLL RESET	When data transmission to the analyzer PLL is completed, this pin goes "high" (Q304 reverses the high and low states of the clock; pin 5 of J303 outputs clock).
13	O	ANALYZER PLL SI	Outputs data to the analyzer PLL (reversed at Q304; pin 5 of J303 outputs clock).
14	I	P25	Unused. Connected to Vcc through R313 to keep the high state.
15	O	A/D CLK	Clock for activating Q302 (clock frequency, about 125 kHz).
16		P27	Outputs when Q301 reads data from Q302. Unused. Left open.
17	I	$\overline{\text{OBF}}$	When Q101 sends a command to Q301, this pin goes "low".
18	I	$\overline{\text{INTR}}$	When Q302 informs the completion of A/D conversion to Q101, this pin goes "low".
19, 20	I	P52, P53	Unused. Connected to Vcc to keep high status.
21		P54	Unused. Left open.
22	I	$\overline{\text{ANALYZER UNLOCK}}$	When the analyzer PLL is unlocked, this pin goes "low". When the analyzer PLL is locked, this pin goes "high".
23, 24		P56, P57	Unused. Left open.
25~32	I/O	P60~P67	NOTE 3
33		Vcc	(+5±0.5)V DC
34~38	O	SUB ADD. 15~11	NOTE 4
39~41		P42~P40	Unused. Left open.
42		Vss	Ground.
43~49		P17~P11	Unused. Left open.
50	O	D/I	When this pin goes "low", pins 51~58 of Q301 control the mode and frequency of Q108 and Q109. When this goes "high", pins 51~58 of Q301 read data displayed on the bandscope.
51~58	I/O	SUB DATA 7~0	NOTE 5
59, 60		P74, P73	Unused. Left open.
61	O	READ/$\overline{\text{WRITE}}$	When data is written to Q108 and Q109, this pin goes "low". When data is read from Q108 and Q109, this pin goes "high".
62	O	$\overline{\text{WR}}$	When voltage on pin 2 of Q301 is A/D converted, this pin goes "low".
63	O	$\overline{\text{RD}}$	When pins 51~58 of Q301 read data from Q302, this pin goes "low".
64	O	E	Synchronous clock for data exchange between Q301 and Q108 and Q109 (clock frequency: 1.0 MHz).
			Writes data to Q108 and Q109 at the emergency of a signal and reads data from Q108 and Q109 while this pin is "high".

5. BLOCK DIAGRAM




SECOND LOCAL
AMP/MIX/VCO
+5V
Q501
TA7358P
PLL IC
Q503
M54927P
X501
4.5MHz
10.7MHz SECOND IF
PD06 FM-N THIRD IF
NOISE DET
Q604,Q605
0A90 x 2
FM-N
SQL
+5V
IF IC
L.P.F. (FM-N)
AF
BUFF
Q601
2SC2714
F601
10.7MHz
Q602
TK10420
X601
10.245MHz
BUFF
Q606
2SC2714
PD08 AUDIO SIGNAL SWITCHING
AF SW
Q801
Q802
Q803
ISI555 x 3
MUTE SW
Q805,Q807
ISI555 x 2
AMP
Q808
2SC2712
DET
Q809,Q810
0A99 x 2
DC SW
Q811
2SC2712
MUTE SW
Q804
2SC2712
MUTE SW
Q014
2SC536
PD07 FM-W/AM DETECTOR
IF SW
Q703
2SC2714
FM-W/AM
DET IC
Q702
BA4220B
L.P.F.
AF(FM-W)
F703
455kHz
F702
455kHz
L.P.F.
AF(AM)
AMP
Q701
2SC2714
F701
10.7MHz
AGC
Q704
2SC2712
MUTE SW
Q705
2SC2712
SQL
FM-W
REG
Q016,Q017
M5236L
2SA1020
PROTE
Q018
USA10G
+9.5V
REG
Q019
7805
+5V
AF PWR AMP
Q027
TA7222AP
SPEAKER
PM02 VOLUME
TONE
CONT.
VOLUME
POWER SW
REG
Q309
TA78008AP
+8V
+5V
+6V
Q305,Q306,Q307
S-8054ALB
TL7705ACPS
TC4S81F
REG
Q311
2SC2655Y
REG
Q310
TA78006AP
+32V
REG
Q314,Q315
HZ6A-1
PC317
Q308
M5231TL
L301
CPS118IN
FM-N/FM-W
FM-W
FM-N/AM
AM
FM-W
FM-N
Q020, Q021
Q022, Q023
Q024, Q025, Q026
RN2206
ISI555
PM05
MODE VOLTAGE MUTE
DC +13.8V IN


P053
077B
079B
061B
W0
W002
061B
080B
079B
025B
024B
026
023B
021B
V101
038B
020B
036B
040B
065B
019B
022B
V102
Q119
042B
027B
017B
032B
029B
042B
040B
043B
037B
PD03
018B
PM02
042B
040B
B101
073B
001B
S101
PD01
005B
006B
040B
007B
008B
041B
009B
076B
J081
041B
012B
012B
039B
PD02
079B
010B
011B
028B
078B
016B
015B
014B
013B


062B
086B
054B 066B
064B
068B
066B
067B
PM01
067B
059B
P051
PM03
063B
060B
066B
085B
PD04
S051
L005
J004
065B
056B
057B
058B
050B
083B
053B
055B
065B
084B
055B
065B
065B
030B
082B
074B W001
075B
074B
075B
H001
073B
072B
071B
070B
079B
081B
078B
002S
004T
003T
002T
001T
009S
006S
011S
005S
001S
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007S
003S
010S
004S
PACKING